MMAGIX™
TECHNOLOGY LIMITED
MULTIMEDIA MULTIPROCESSOR SUPERCOMPUTER
CHIP TECHNOLOGY

MMAGIX IP CORE DESIGN PRODUCT ANNOUNCEMENT

NEW 6 ISSUE SMT 64 BIT SUPERCOMPUTER IP CORE FOR TELECOMS, MILITARY, AEROSPACE, MEDICAL & INDUSTRIAL SYSTEMS.

- 1+ BIPS performance on Virtex-XC5VLX110T FPGA
- Symmetric Multithreading at 5-6 instructions/cycle
- Multiport Cache Memory allows 6 instruction issue
- SMT absorbs latency on Cache Memory Miss
- 8/16/32/64/128 bit Integer, 32/64 bit Floating Point
- 128 bit SIMD Vector, Matrix & String processing
- Fast Multiply/MAC and Fast Divide/Remainder/Sqrt
- Signed/unsigned Overflow Saturation Arithmetic
- 16 & 32 bit instruction formats for space & speed
- Optimized for efficient compilation of C, C++, Java
- Zero cycle looping for maximum performance
- High bandwidth Superconnectivity direct to Cache
- 1 Gb/s Ethernet and 10 Gb/s SPI-4.2 direct to Cache
- There is no comparable IP Core on FPGA

"That's phenomenal!" **- Dr Bart Stuck, 30 April 2008.**

MMAGIX IP Core Design Product Anouncement:

MMAGIX Technology Limited is delighted to announce the success of its R&D program in developing an IP Core that can achieve greater than 1 Billion Instructions Per Second (1+ BIPS) sustained Supercomputer performance in the Xilinx Virtex-5 FPGA range by means of up to 6 simultaneous instruction issue Symmetric Multithreading (SMT) at a system clock frequency over 200MHz. The MMAGIX Architecture efficiently scales to multiple IP Cores on larger FPGAs and on ASIC in the future.

MMAGIX is a US and foreign Patent Pending (1,600+ claims) SMT Supercomputer IP Core Architecture, Instruction Set and Design that will deliver the most advanced supercomputing and superconnectivity for true digital convergence in Multimedia processing, with:

- **Supercomputer performance for Telecoms, Military & Aerospace, Medical, Industrial and Entertainment systems.**
- **Simultaneous execution of multiple high speed programs with multiple high speed data streams in real time.**
- **Multiple Multithreading IP Cores to provide real time simultaneous multiprocessing of Multichannel Data, Voice & Video.**
- **Up to 6 simultaneous instruction issue Symmetric Multi-Threading (SMT) per IP Core.**
- **No other IP Core of anywhere near this performance level is available on FPGA.**
- **MMAGIX will supply licensable reference designs to support Product Development Engineers to develop innovative products using MMAGIX IP Cores.**
- **MMAGIX is a Green energy saving technology for the 21st Century.**

FPGAs are highly suited to Telecoms, Military & Aerospace use and the MMAGIX Architecture is perfect for their needs, delivering an unprecedented combination of real time simultaneous multithreading supercomputer performance and ultra high bandwidth interface superconnectivity, combined with customizable and upgradeable interface hardware.

The MMAGIX Architecture has multiple 64/128 bit Arithmetic Logic Units (ALUs) which support SIMD Scalar and Vector Instructions on 8, 16, 32, 64 and 128 bit data, executing SIMD text string instructions 16 bytes at a time. 32 and 64 bit Floating Point instructions are supported with SIMD operations 128 bits at a time.

The MMAGIX Architecture features ultra high bandwidth Superconnectivity to high speed peripherals by direct buffering in dual port BRAM/SRAM memory integrated with the L2 Data Cache, supporting 2x10 Gb/s SPI-4.2 serial Telecommunications data ports in a Virtex-XC5VLX110T FPGA.

The MMAGIX SMT Core achieves multiport 2R2W access to its Registers and Caches by clocking the FPGA BRAMs at double the system clock frequency.

As in some cycles resource competition means that less than 6 instructions are available to execute, sustained performance is slightly lower at around 5.5 instructions per cycle, but the SMT Architecture absorbs the latency of memory access, eliminating pipeline stalls and bubbles. The IP Core can be made optionally with 2-6 SMT issue pipelines and with different Cache sizes, for different performance/cost tradeoffs.

There are ample logic resources to enable the addition of an efficient line-speed hardware encryption/decryption accelerator for AES or other standards. There is also the capability to add specialized super high speed digital signal processing and other custom hardware such as Telecommunications Switching in the FPGA.

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